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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/488,909	01/21/2000	Hideki Hiura	P4010NP/CSL	5094

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EXAMINER	
HOANG, PHUONG N	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/488,909	HIURA ET AL.	
	Examiner	Art Unit	
	Phuong N. Hoang	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 21 are pending for examination.

2. This office action is in response to amendment filed 7/5/06.

3. References, not found in this office action, can be found in previous office actions.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 – 11, and 15 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hetherington, US patent no. 6,275,810 in view of Kaufman, US patent no. 5,313,647.

6. **As to clam 1**, Hetherington teaches a method for providing for concurrent subprocessing of a master process, the method comprising the steps of:

interfacing with a master process (daemon, col. 1 lines 25 – 30 and col. 5) when a user-specific operation (endpoint computer running locale application, col. 4 - 5) is encountered (interfacing when a specific locale is selected, col. 6 lines 58 – 67);

mapping a user-specific process with the master process (specify the locale to be mapped, col. 4 lines 49 – 65 and col. 6 lines 58 - 67);

processing the user-specific operation in the user-specific process (running the endpoint application, col. 5 lines 25 – 67).

Hetherington does not explicitly teach the step of mapping so that it overlays virtual addresses of the master process. However, Hetherington teaches that the global process spawns the user-specific process (daemon spawns multiple processes, col. 1 lines 25 – 30 and col. 4). One of ordinary skill in the art would understand that when spawning, the child process would inherent all the property of the parent process.

Kaufman teaches that when spawning, the child would overlay the parent's virtual memory address (vm_folk to duplicate a parent process's virtual memory information for a child process, mapin the context address which would translate and references to virtual address for accessing data, col. 18 lines 28 – 55, col. 31 lines 14 – 65 and col. 34 lines 10 - 15 and col. 2 lines 1 – 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching Hetherington and Kaufman's system because Kaufman's duplicating virtual memory address in the spawning process would let the child process virtual address overlays the parent's process virtual address when

it inherits all property of the parent's process to have an identical or mirror address of the parent.

7. **As to claim 2**, Hetherington teaches the steps comprising the step of transferring data between the master process and the user-specific process (mapping, col. 4 lines 50 – 65 and col. 6 lines 58 – 65) using a communication channel that does not require the serialization of data (IPC facility 19, col. 12 – 20).

8. **As to claim 3**, Hetherington modified by Kaufman teaches the step of providing an interface (Hetherington; map, col. 4 lines 50 – 65 and col. 6 lines 58 – 65) for the user-specific process that mirrors (Kaufman; duplicate, col. 31 lines 14 – 20) an interface for the master process.

9. **As to claim 4**, Hetherington teaches the steps of wherein the master process is a global locale process (daemon containing multiple locales, col. 6) and the user-specific process is a locale-specific process (endpoint application running locale-specific, col. 6).

10. **As to claim 5**, Hetherington teaches the step of wherein the user-specific process is mapped after the user-specific operation is encountered (mapped when user specifies the locale, col. 6 lines 58 – 65).

11. **As to claim 6**, Hetherington teaches the step of wherein the user-specific process is mapped before the user-specific operation is encountered (the default locale, col. 6 lines 10 – 25).

12. **As to claim 7,** Hetherington teaches the step of returning processing to the master process after processing the user-specific operation in the user-specific process (the server maintains the mapping process, col. 4 lines 50 – 67).

13. **As to claim 8,** it is the medium claim of claim 1. See rejection for claim 1 above. Further, Hetherington teaches the step of mapping a plurality of concurrent user-specific processes (Gregorian, Hijri, and Hebrew may be selected and mapped, col. 6 lines 58 – 67 and col. 4 lines 49 – 65) to the global process.

14. **As to claim 9,** Hetherington teaches the instructions (instructions, col. 15 lines 60 – 65), when executed, provide each of the plurality of concurrent user-specific processes with an interface that is identical to an interface of the global process.

15. **As to claim 10**, Hetherington modified by Kaufman teaches the steps of mapping sub-processes within each of the plurality of user-specific processes, the sub-processes being mapped to virtual addresses that are equivalent to virtual addresses (vm_folk to duplicate a parent process's virtual memory information for a child process,

col. 31 lines 14 – 20 and col. 2 lines 1 – 5) for user-specific operations of the global process.

16. **As to claim 11**, Hetherington teaches the step of returning processing to the global process after execution of the sub-processes is complete (the server maintains the mapping process, col. 4 lines 50 – 67).

17. **As to claim 15**, it is the apparatus claim of claim 1. See rejection for claim 1 above.

18. **As to claims 16 – 21**, see rejection for claims 2 – 7 above.

19. Claims 12 - 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaufman, US patent no. 5,313,647 in view of Hetherington, US patent no. 6,275,810.

20. **As to claim 12**, Kaufman teaches a computer system for enabling concurrent multiple sub-process handling in a global process environment, the system comprising the steps of:

A memory (col. 4 lines 50 – 60);

a global process (parent process, col. 31 lines 15 – 20); and

a virtual memory separator (vm_folk to duplicate a parent process's virtual memory information for a child process, col. 31 lines 14 – 65, col. 34 lines 10 – 15, and col. 2 lines 1 – 5) that maps a child process to virtual addresses that mirror virtual addresses of the global process, the child process having an interface that mirrors an interface of the global process.

A processor (digital data processor, col. 3 lines 32 – 40).

Kaufman does not explicitly teach that the child process is a user-specific process.

Hetherington teaches that the child process is a user-specific process (endpoint running locale application, col. 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching Kaufman and Hetherington's teaching because Hetherington's user-specific process would provide the child process to run on an application having user-specific environment.

21. **As to claim 13**, Hetherington teaches the step of wherein the global process is a global locale process (daemon contains all locales, col. 5) and wherein the user-specific process is a locale-specific process (endpoint application is locale application, col. 5).

22. **As to claim 14,** Hetherington teaches the step of wherein the global process is a global daemon process (daemon spawns multiple processes, col. 1 lines 25 – 30) and

wherein the user-specific process is a user-specific daemon process (each endpoint contains a daemon, col. 4 lines 50 - col. 5 lines10).

Response to Arguments

23. Applicant's arguments filed 7/5/06 have been fully considered but they are not persuasive.

24. Applicant argued in substance that

(1) VM_MAPOUT, the VM_MAPIN maps context address, not virtual address, and VM_FOLK is to remove explicit assignment of the system virtual address for the child. Mapin the overlay object would be different "overlay" as used in the claim.

25. Examiner respectfully disagrees with applicant's remark.

As to point 1, the memory address consists of virtual address and context address. System virtual address stores the data from context address, and vm_mapin the context address which would translate and references to virtual address when accessing data, so mapping context address would also map virtual address, col. 18 lines 28 – 55, col. 31 lines 14 – 65 and col. 33 lines 1 – 65, col. 34 lines 10 - 15 and col. 2 lines 1 – 5). The cited the paragraph should be read as a whole, VM_FORK duplicate a parent process's virtual memory information (col. 31 lines 15 – 17), the duplication would remove the child virtual

memory, so the child would get the same virtual memory information of the parent. The mapping overlay object is one function of the mapin process.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong N. Hoang whose telephone number is (571)272-3763. The examiner can normally be reached on Monday - Friday 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on 571-272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ph
September 6, 2006

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER